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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/792,153	03/02/2004	Robert E. Eccles	X-1270 US	4867

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XILINX, INC
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EXAMINER	
KIK, PHALLAKA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/792,153	ECCLES, ROBERT E.	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2004 and 28 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25* is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☒ Claim(s) *26-31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/2/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to the Application and IDS filed on 3/2/2004, and Application Data Sheets filed on 3/2/2004 and 6/28/2004. Claims 1-31 are pending.

Priority

2. If applicant desires to claim the benefit of a prior-filed application under 35 U.S.C. 120, a specific reference to the prior-filed application in compliance with 37 CFR 1.78(a) must be included in the first sentence(s) of the specification following the title or in an application data sheet. For benefit claims under 35 U.S.C. 120, 121 or 365(c), the reference must include the relationship (i.e., continuation, divisional, or continuation-in-part) of the applications.

If the instant application is a utility or plant application filed under 35 U.S.C. 111(a) on or after November 29, 2000, the specific reference must be submitted during the pendency of the application and within the later of four months from the actual filing date of the application or sixteen months from the filing date of the prior application. If the application is a utility or plant application which entered the national stage from an international application filed on or after November 29, 2000, after compliance with 35 U.S.C. 371, the specific reference must be submitted during the pendency of the application and within the later of four months from the date on which the national stage commenced under 35 U.S.C. 371(b) or (f) or sixteen months from the filing date of the prior application. See 37 CFR 1.78(a)(2)(ii) and (a)(5)(ii). This time period is not extendable and a failure to submit the reference required by 35 U.S.C. 119(e) and/or 120, where applicable, within this time period is considered a waiver of any benefit of

such prior application(s) under 35 U.S.C. 119(e), 120, 121 and 365(c). A benefit claim filed after the required time period may be accepted if it is accompanied by a grantable petition to accept an unintentionally delayed benefit claim under 35 U.S.C. 119(e), 120, 121 and 365(c). The petition must be accompanied by (1) the reference required by 35 U.S.C. 120 or 119(e) and 37 CFR 1.78(a)(2) or (a)(5) to the prior application (unless previously submitted), (2) a surcharge under 37 CFR 1.17(t), and (3) a statement that the entire delay between the date the claim was due under 37 CFR 1.78(a)(2) or (a)(5) and the date the claim was filed was unintentional. The Director may require additional information where there is a question whether the delay was unintentional. The petition should be addressed to: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

If the reference to the prior application was previously submitted within the time period set forth in 37 CFR 1.78(a), but not in the first sentence(s) of the specification or an application data sheet (ADS) as required by 37 CFR 1.78(a) (e.g., if the reference was submitted in an oath or declaration or the application transmittal letter), and the information concerning the benefit claim was recognized by the Office as shown by its inclusion on the first filing receipt, the petition under 37 CFR 1.78(a) and the surcharge under 37 CFR 1.17(t) are not required. Applicant is still required to submit the reference in compliance with 37 CFR 1.78(a) by filing an amendment to the first sentence(s) of the specification or an ADS. See MPEP § 201.11.

3. **It is noted that Applicant has filed ADS on 3/2/2004 and 6/28/2004, claiming priority as a continuation of the provisional application No. 60/425,143. However,**

this provisional application is incorrect. The correct number should be 60/452,143. Applicant is required to make proper correction as noted above in order to obtain this priority.

Specification

4. The disclosure is objected to because of the following informalities:

The attempt to incorporate subject matter into this application by reference to the "Verilog Language Reference Manual (LRM) found at http://www-ee.eng.hawaii.edu/-msmith/Aslcs/HTML/verilog/verilog.htm" is ineffective because hyperlink is not permitted in the incorporation by reference (see MPEP 608,01(p); 37 CFR 1.57(d)).

Appropriate correction is required.

5. The incorporation by reference will not be effective until correction is made to comply with 37 CFR 1.57(b), (c), or (d). If the incorporated material is relied upon to meet any outstanding objection, rejection, or other requirement imposed by the Office, the correction must be made within any time period set by the Office for responding to the objection, rejection, or other requirement for the incorporation to be effective. Compliance will not be held in abeyance with respect to responding to the objection, rejection, or other requirement for the incorporation to be effective. In no case may the correction be made later than the close of prosecution as defined in 37 CFR 1.114(b), or abandonment of the application, whichever occurs earlier.

6. Any correction inserting material by amendment that was previously incorporated by reference must be accompanied by a statement that the material being inserted is

the material incorporated by reference and the amendment contains no new matter. 37 CFR 1.57(f).

Claim Objections

7. **Claims 5-12,26-31** are objected to because of the following informalities:

As per **claim 5**, "state statements" (lines 14 and 17) should be --states-- for proper antecedent basis.

As per **claim 11**, "state statements" (lines 3 and 7) should be --states-- for proper antecedent basis.

As per **claims 6-12**, the claims are also objected to for incorporating the above errors into the respective claims by claim dependency.

As per **claim 16**, --further-- should be inserted before "comprises" (line 2) to define the further limitations.

As per **claim 26**, "the other" (lines 3 and 7) should be --other-- for proper antecedent basis.

As per **claims 27-31**, the claims are also objected to for incorporating the above errors into the respective claims by claim dependency.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the

applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. **Claims 1, 2-4,18-21** are rejected under 35 U.S.C. 102(e) as being anticipated by anticipated by **Guccione et al.** (U.S. Patent No. 6,668,237).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per **claims 1,18-19**, all of the elements of the claims are discussed in col. 2, lines 27-39, wherein the reconfiguration test program corresponds to the at least one test patterned obtained to test the at least programmable logic portion, wherein the configuration bitstream corresponds to the memory states for configuring the programmable logic device, wherein the applying the memory states to at least the programmable logic portion corresponds to the configuring of the PLD using the bitstream data, and wherein the equivalency checking is part of the comparison of the expected results and the result data being read back from the PLD (see also col. 1, lines 17-27), wherein the system, mass storage memory, computer, processor, i/o interface, databases and tools are part of the computer-implemented method/system as

illustrated in Fig. 1, being necessary to implement the computer-implemented method/system, wherein the various processes (i.e., equivalency checking, obtaining of memory states) can also be implemented as with the system/method as a routine or as a call to a separate software tool, as is known in the art.

As per **claims 2-3**, all of the elements of claim 1, from which the claims depend, are discussed in the rejection of claim 1 above, wherein the filtering, combining, configuring sub-block and storing are part of the tracking and changing the portions of the configuration so that only the selected sections of the programmable device that need to be configured, are configured (see col. 3, lines 4-17, 33-35).

As per **claim 4**, all of the elements of claim 1, from which the claim depends, are discussed in the rejection of claim 1 above, wherein the equivalency checking is done at a Boolean level is described in col. 4, lines 11-29 (i.e., bit-wise comparison using Boolean logic as shown in the program such as "!=").

As per **claims 20-21**, all of the elements of the claims are discussed in the rejection of claims 1 and 2 above, the first, second and subsequent portions correspond to the selected portions of the programmable device for which the configuration are selectively or partially changed and applied, wherein the level abstract in this case is at least the configuration data bit abstract.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious

> at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. **Claims 5-16,22-24** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Guccione et al.** (U.S. Patent No. 6,668,237) in view of **Agrawal et al.** (U.S. Patent No. 6,216,257).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

As per **claims 5-10,13,15-16,22-24**, **Guccione et al.** teach the obtaining of the states, applying of the memory states for configuring the portion of the design, and equivalency checking, as discussed in the rejection of claims 1,20 above, wherein the bitstream is a form of the memory states which has been mapped and translated into

the target format, wherein the use of database or file for storing the unconfigured design and test pattern is part of the computer-implemented method/system (see Fig. 1), being necessary to implement the computer-implemented method/system. However, **Guccione et al.** failed to specifically teach that the memory states (i.e., configuration data such as bitstream) are the results of the placer and router previously performed or synthesized, including prior to a level abstraction (i.e., configuration data abstraction) and after the level abstraction. **Agrawal et al.** teach the use of placer and router and logic synthesizer (being performed before and after the level abstraction) being performed on the circuit design at a higher level, such as HDL, register transfer level, so that the resources available on the programmable devices are optimized, from which the configuration bitstream data is generated, for configuring the programmable logic devices (see col. 1, lines 60-67; col. 13, line 63 to col. 14, line 33; Fig. 1A). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further incorporate the place and router and/or synthesizer as taught by **Agrawal et al.** into the method/system of **Guccione et al.** because such incorporation would further allow the circuit design to be optimized, while providing the necessary configuration data as needed by the method/system of **Guccione et al.** to implement the circuit so that the programmable logic device functions can checked.

As per **claim 14**, all of the elements of claim 13, from which the claim depends are discussed in the rejection of claim 13 above, wherein the hierarchical assembling of the test patterns is also taught by **Guccione et al.** as part of the tracking and changing the portions of the configuration so that only the selected sections of the programmable

device that need to be configured, are configured, which necessarily involves some sort of hierarchical assembling or combining since at least different portions of the circuit configuration corresponds to different hierarchical circuit description (see col. 3, lines 4-17, 33-35).

As per **claims 11-12**, all of the elements of claim 5, from which the claim depends are discussed in the rejection of claim 13 above, wherein the further limitations are also taught by **Guccione et al.** as discussed in the rejection of claims 2-3 above.

12. **Claim 17** is rejected under 35 U.S.C. 103(a) as being obvious over **Guccione et al.** (U.S. Patent No. 6,668,237) in view of **Huggins et al.** (U.S. patent application publication no. 2003/0200520).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing

that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

As per **claim 17**, **Guccione et al.** disclose all of the elements of claim 13, from which the claim depends are discussed in the rejection of claim 13 above, but failed to teach that the equivalency checker is configurable to operate at a level of abstraction selected from transistor, gate, register transfer, behavioral and system levels. **Huggins et al.** teach the an equivalency checker which involves the use of translating or converting the configuration data (i.e., bitstream) into higher circuit description levels (i.e., behavioral or gate levels) so that verification for equivalence can be made (see paragraph [0022]; Fig. 4). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further incorporate the equivalence checker of **Huggins et al.** having various levels of comparisons, into the system/method of **Guccione et al.** because such incorporation would allow the programmable devices to be checked for proper operation at the higher levels of circuit abstractions having the benefits associated with higher levels of circuit abstractions (i.e., at least the designer can readily identify which circuit element(s) are functional and which ones are not) while performing the desired functional verification as taught by **Guccione et al.**.

Allowable Subject Matter

13. **Claim 25** is allowed.

14. **Claims 26-31** would be allowable if rewritten or amended to overcome the minor informalities objections, set forth in this Office action.

15. The following is a statement of reasons for the indication of allowable subject matter:

As per **claims 25-31**, the independent claim 25, from which the respective claims depend, recites the method of checking whether a programmable logic device functions properly when configured, comprising the inventive steps of renaming the cell of the logic block, in combination with the steps of filtering, translating, and parsing as claimed, which the prior arts made of record failed to teach or suggest. In particular, the various prior arts made of record teach various methods/systems for verifying the proper functionality of the programmable devices, including the use of renaming cells or elements (see prior arts cited above and **Poznanovic et al.**, U.S. patent application publication no. 2006/0041872, especially paragraphs [0012]-[0016], [0150]). Accordingly, the claimed invention is novel and un-obvious over the prior arts made of record.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicant is requested herein to consider them carefully in response to this Office Action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Monday-Thursday, 6:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

571-273-8300

Phallaka Kik
U.S. Patent Examiner
March 24, 2006